What is claimed is:

1. A processing system comprising:

dispersal logic to receive a plurality of instructions;

an execution port coupled to said dispersal logic; and

a No-op port coupled to said dispersal logic.

2. The system of claim 1 wherein said No-op port is to process NOP instructions of said plurality of instructions.

3. The system of claim 2 wherein said execution port is to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

4. A processing system comprising:

dispersal logic to receive a plurality of instructions;

a plurality of execution ports coupled to dispersal logic; and

a No-op port coupled to said dispersal logic, said No-op port to process NOP instructions of said plurality of instructions.

5. The system of claim 4, wherein said plurality of instructions are taken from at least two individual threads.

6. The system of claim 5 further comprising:

first and second instruction buffers coupled to said dispersal logic to store said plurality of instructions for first and second threads, respectively.

7. The system of claim 4, wherein said execution ports are to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

8. The system of claim 6, wherein said execution ports are to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

9. The system of claim 7 wherein said plurality of instructions are grouped into bundles prior to processing in said No-op and execution ports.

10. The system of claim 8 wherein said plurality of instructions are grouped into bundles prior to processing in said No-op and execution ports.

11. A method of dispersing instructions in a multi-threaded processing system including a plurality of execution ports and at least one NO-op port, comprising:

determining if an instruction is a NOP instruction; and

dispersing said NOP instruction for execution by a No-op port.

12. The method of claim 11, wherein said plurality of instructions are taken from at least two individual threads.

13. The method of claim 12 further comprising:

supplying said plurality of instructions to said dispersal logic from first and second instruction buffers coupled to dispersal logic to store said plurality of instructions for first and second threads, respectively.

14. The method of claim 11, further comprising:

processing instructions in said execution ports wherein said execution ports are to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

15. The method of claim 13, further comprising

processing instructions in said execution ports wherein said execution ports are to process at least one of the following: memory instructions, integer instructions, floating-point instructions, and a branch instructions.

16. The method of claim 14 further comprising:

grouping said plurality of instructions into bundles prior to said supplying said instructions to said dispersal logic.

17. The method of claim 15 further comprising:

grouping said plurality of instructions into bundles prior to said supplying said instructions to said dispersal logic.